



Gen-Z[™] Memory Module (ZMM)

SMART Modular's Gen-Z scalable computing interconnect protocol provides a simplified interface based on memory semantics and is designed to handle advance workloads, enabling data centric computing with scalable memory pools and resources for real-time analytics and in memory applications. The Gen-Z standard was developed to enable new solution architectures for delivering high levels of performance (high-bandwidth, low-latency), software efficiency, power optimizations, and industry agility.

Product Description

- Gen-Z Form Factor 4C-SFF-TA-1008/9 (EDSFF 3-inch form factor compliant)
- Available in 64GB capacity of dual rank DDR4 memory with ECC
- Available in user-programmable FPGA variant to allow adding custom logic for differentiation, or add hardware engines in FPGA, which can offload specific functions to memory module, right next to where data resides.

Why the ZMM?

- New Type of Design Challenges
 - The increase in number of CPU cores has not been matched by an increase in memory bandwidth leading to memory bandwidth starved CPU cores. By being able to support more memory interfaces and memory modules Gen-Z serial attached ZMM memory increases memory bandwidth per core increasing system performance.
 - Gen-Z ZMM memory provides load-store direct addressing to memory by applications eliminating operating system and device driver overhead. CPU cores spend more time executing end applications.
- Workloads Are Changing
 - Latest HPC models and Al/ML algorithms require large pool of memory to store intermediate
 data sets. These data sets require concurrent access from multiple compute nodes. Thus such
 workloads need large pool of shared memory, independent of any compute node.
- New Generation of Hardware
 - As network speeds are increasing, the latency difference between local attached memory and remotely accessible memory is decreasing. Addition of specialized hardware accelerators.



Features & Benefits

- Multiple Access Semantics Support (Byte and Block Addressable DRAM Access, In-Band Configuration, Access Key/Region Key Memory Isolation Opcodes)
- Gen-Z Phy Support (16 Total Links 4x, 4-Lane Links, 802.3 25Gbps), with 4 Requestor and 4 Responder Configuration
- Write Command Collision Detection and Ordering Logic with Support for 9 to 11 Cycles of CAS Write Latency at 2400 MTS
- Media Scrubbing (Background ECC Detection and Correction)
- Gen-Z Lane Reduction Support

Applications

- In-Memory Analytics
- Similarity Search
- Large-Scale Graph Inference
- Financial Modeling

Ordering Information

SMART Part Number	Density	Form Factor	Device Config
Gen-ZTM Memory Module (ZMM)			
STZAB64G7B4S36HA	64GB	Gen-Z 3.0" Form Factor 4C-SFF-TA-1008/9 (104.90 x 76.00 x 16.80mm)	(x64 +8) dual rank DDR4

Transforms Performance



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